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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
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09/537,274 03/29/00 MOSLEY

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021186 MMC2/1107  
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EXAMINER

THOMAS E

ART UNIT

PAPER NUMBER

2831

DATE MAILED:

11/07/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trad marks

# Office Action Summary

Application No.

09/537,274

Applicant(s)

MOSLEY, LARRY EUGENE

Examiner

Eric W Thomas

Art Unit

2831

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 20 August 2001.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☒ The proposed drawing correction filed on 20 August 2001 is: a) ☒ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other:

## DETAILED ACTION

### Introduction:

The examiner acknowledges, as recommended in M.P.E.P., the applicant's submission of the amendment dated 8/20/01. At this point, claims 1, 4-6, 9-14, 17-21 have been amended. Claims 1-21 are pending in the instant application.

### ***Claim Rejections - 35 USC § 102***

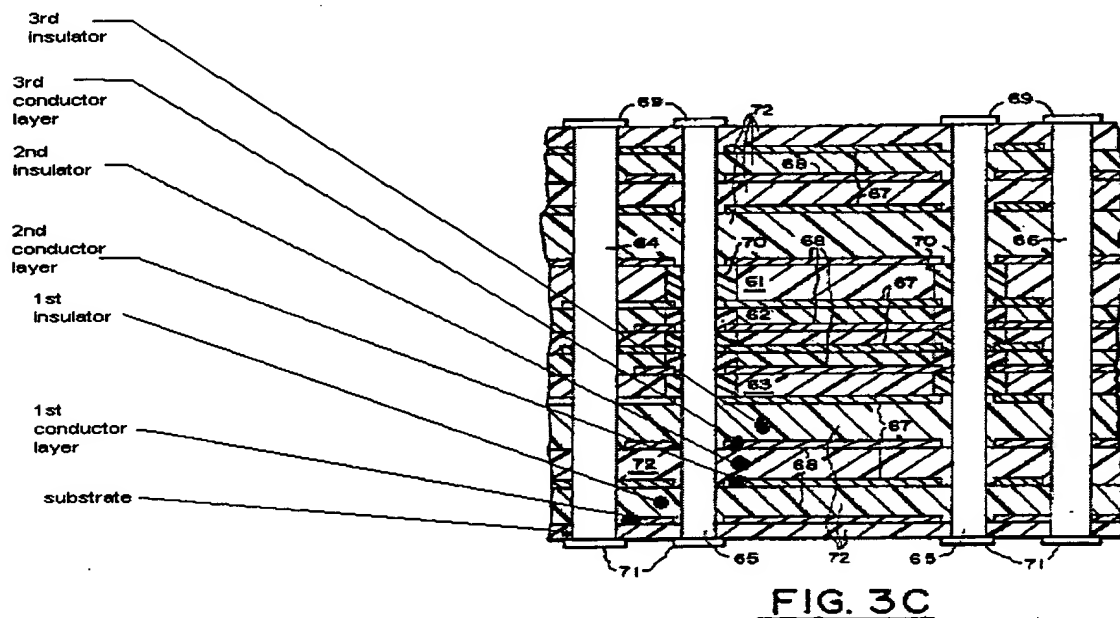
The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1, 2, 14-16, & 19, are rejected under 35 U.S.C. 102(e) as being anticipated by Farooq et al (US 6,072,690).



Regarding claim 1, Farooq et al. disclose in fig. 3C, a multilayer integrated circuit capacitor comprising: a substrate<sup>1</sup> (72); a first conductive layer (68) located over the substrate; a first insulator layer (72) located over the first conductive layer; a second conductive layer (67) located over the first insulator layer; a second insulator layer (72) located over the second conductive layer; a third conductive layer (68) located over the second insulator layer; a third insulator layer (72) located over the third conductor layer; and a plurality of conductive vias (64, 66) downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductor layers.

Regarding claim 2, Farooq et al. further comprises a plurality of controlled collapse chip connection (C4) lands fabricated on the third insulator layer and in electrical contact with the plurality of conductive vias (col. 3 lines 25-30).

Regarding claim 14, Farooq et al. disclose in fig. 1, & 3C, a circuit board (col. 2 lines 1-7) having supply voltage interconnect (col. 3 lines 3-12) lines; a first integrated circuit die mounted on a circuit package (see fig. 1) a second integrated die mounted on the circuit and electrically connected to the supply voltage interconnect lines, the second integrated circuit package comprises a capacitor comprising: a substrate (72); a first conductive layer (68) located over the substrate; a first insulator layer (72) located over the first conductive layer; a second conductive layer (67) located over the first insulator layer; a second insulator layer (72) located over the second conductive layer; a third conductive layer (68) located over the second insulator layer; a third insulator layer

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<sup>1</sup> An underlying layer; a substratum. *The American Heritage® Dictionary of the English Language, Third Edition* copyright © 1992 by Houghton Mifflin Company

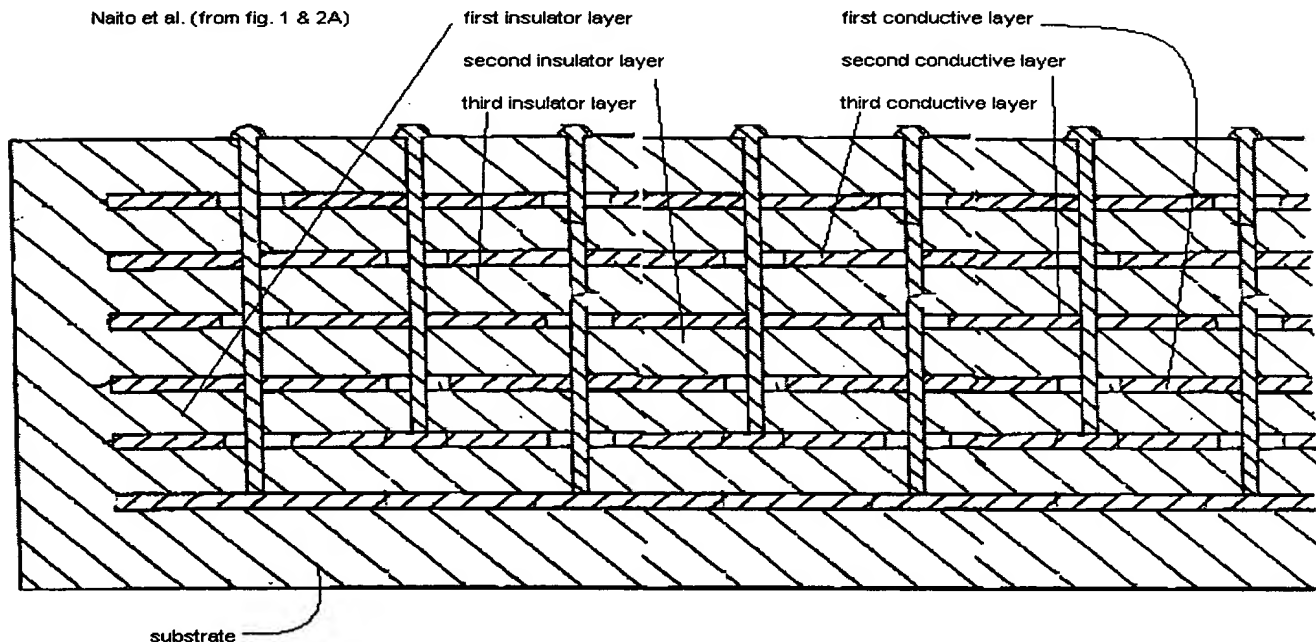
(72) located over the third conductor layer; and a plurality of conductive vias (64, 66) downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductor layers.

Regarding claim 15, Farooq et al. further comprises a plurality of controlled collapse chip connection (C4) lands fabricated on the third insulator layer and in electrical contact with the plurality of conductive vias (col. 3 lines 25-30).

Regarding claim 16, Farooq disclose the first integrated circuit package is a processor (see col. 1 lines 11-65 – col. 2 lines 1-67, col 3 lines 1-50; & fig. 1).

Regarding claim 19, Farooq et al. disclose in fig. 3C, a multi layer integrated circuit capacitor comprising: a substrate (72); a first conductive layer (68) located over the substrate; a first insulator layer (72) located over the first conductive layer; a second conductive layer (67) located over the first insulator layer; a second insulator layer (72) located over the second conductive layer; a third conductive layer (68) located over the second insulator layer; a third insulator layer (72) located over the third conductive layer; and a plurality of conductive vias (64, 66) downwardly extending through the third insulator layer to provide electrical interconnection to the first, second and third conductive layers, the plurality of conductive vias further extending through the substrate to provide electrical interconnects on both a top and a bottom surface of the integrated circuit capacitor.

Claims 1, 8, 11 are rejected under 35 U.S.C. 102(e) as being anticipated by Naito et al. (EP 0, 917,165 A2).



Naito et al. disclose in fig. 1 & 2, a multilayer integrated circuit capacitor comprising: a substrate; a first conductive layer (33) located over the substrate; a first insulator layer (32) located over the first conductive layer; a second conductive layer (34) located over the first insulator layer; a second insulator layer (32) located over the second conductive layer; a third conductive layer (33) located over the second insulator layer; a third insulator layer (32) located over the third conductor layer; and a plurality of conductive vias (40,41) downwardly extending through the third insulator layer to provide electrical interconnect to the first, second and third conductor layers.

Regarding claim 8, some of the plurality of conductive vias (40) pass through the second conductive layer without forming an electrical connection with the second conductive layer.

Regarding claim 11, Naito et al. disclose in fig. 1 & 2, a multi layer integrated circuit capacitor comprising: a substrate; a first conductive layer (34) located over the substrate; a first insulator layer (32) located over the first conductive layer; a second conductive layer (33) located over the first insulator layer; a second insulator layer (32) located over the second conductive layer; a third conductive layer (34) located over the second insulator layer; a third insulator layer (32) located over the third conductive layer; a first plurality of conductive vias (41) downwardly extending through the third insulator layer, third conductive layer, second insulator layer, second conductive layer and the first insulator layer to provide electrical interconnect to the first and third conductive layers; and a second plurality of conductive vias (40) downwardly extending through the third insulator layer, third conductive layer and second insulator layer to provide electrical interconnect to the second conductive layer.

Claims 1, 7, & 9 are rejected under 35 U.S.C. 102(b) as being anticipated by Watt (US 5,745,335).

Regarding claim 1, Watt discloses in fig. 1, a multilayer integrated circuit capacitor comprising: a substrate (1, 2); a first conductive layer (7) located over the substrate; a first insulator layer (22b) located over the first conductive layer; a second conductive layer (8) located over the first insulator layer; a second insulator layer (24b) located over the second conductive layer; a third conductive layer (9) located over the second insulator layer; a third insulator layer (10) located over the third conductor layer; and a plurality of conductive vias (40, 38, 46) downwardly extending through the third

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insulator layer to provide electrical interconnect to the first, second and third conductor layers.

Regarding claim 7, the second and third conductive layers are fabricated in a plurality of strips, such that a surface area of the second conductive layer is less than a surface area of the first conductive layer and a surface area of the third conductive layer is less than the surface area of the second conductive layer.

Regarding claim 9, Watt discloses in fig. 1 (5-6 – fig. 5 & 6 illustrates two conductor layers), a multilayer integrated circuit capacitor comprising: a substrate (1, 2); a first conductive layer (7) located over the substrate; a first insulator layer (22b) located over the first conductive layer; a second conductive layer (8) located over the first insulator layer; (as seen in fig. 5-6) the second conductive layer is fabricated as a plurality of laterally spaced strips such that a surface area of the second conductive layer is less than a surface area of the first conductive layer; a second insulator layer (24b) located over the second conductive layer; a third conductive layer (9) located over the second insulator layer; the third conductive layer is fabricated as a plurality of laterally spaced strips such that a surface area of the third conductive layer is less than the surface area of the second conductive layer; a third insulator layer (10) located over the third conductor layer; and a first plurality of conductive vias (40 & as seen in the 3<sup>rd</sup> drawing of fig. 5) downwardly extending through the third insulator layer to provide electrical interconnect to the third conductor layers; a second plurality of conductive vias (38 & as seen in the 3<sup>rd</sup> drawing of fig. 5) downwardly extending through the third insulator layer to provide electrical interconnect to second conductor layer; a third



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plurality of conductive vias (46 & as seen in the 3<sup>rd</sup> drawing of fig. 5) downwardly extending through the third insulator layer to provide electrical interconnect to the first conductor layers.

### ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 2-3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naito et al. (EP 0, 917,165 A2) in view of Farooq et al. (US 6,072,690).

Regarding claim 2, Naito et al. disclose the claimed invention except for the C4 lands in electrical contact with the plurality of vias. Farooq et al. teach the use of C4 lands in multilayer integrated circuit capacitors. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form C4 lands on the capacitor of Naito et al. (in which the C4 lands electrically connect the plurality of vias), since such a modification (is well known in the art) would prevent the capacitor from collapsing onto the high frequency circuit board during the connection phase.

Regarding claim 3, Naito et al. disclose in fig. 2, the C4 lands are fabricated in staggered columns in a plan view.

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Claims 4-5, 13, & 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Naito et al. (EP 0, 917,165 A2)

Regarding claim 4 (& 21), Naito et al. disclose the claimed invention except for the insulators are fabricated by a BaSrTiO<sub>3</sub> material. BaSrTiO<sub>3</sub> is a well known dielectric (insulator) used in the capacitor art. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the insulators of Naito et al. using BaSrTiO<sub>3</sub>, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding claim 5, Naito et al. disclose the claimed invention except for the metal conductors are fabricated from a copper material. Copper is a well known material used as conductors in the capacitor art. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the conductors of Naito et al. using a copper material, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Regarding claim 13, Naito et al. disclose the claimed invention except for the insulators are fabricated by a BaSrTiO<sub>3</sub> material. BaSrTiO<sub>3</sub> is a well known dielectric (insulator) used in the capacitor art. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the insulators of Naito et al. using BaSrTiO<sub>3</sub>, since it has been held to be within the general skill of a worker in the

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art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

Claims 6, 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watt (US 5,745,335) in view of Yach et al. (US 6,225,678).

Watt discloses the claimed invention, except for the fourth conductive layer located over the third insulator layer, the fourth conductive layer is patterned to form interconnected lines the selectively connect the plurality of conductive vias. Yach et al. teach a plurality of capacitors can be connected through a interconnect line. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form an interconnect to connect a plurality of Watt capacitors; since such a modification would connect a plurality of like capacitors together providing a particular capacitance for a system.

Regarding claim 10, Watt discloses the claimed invention except for a fourth conductive layer located over the third insulator layer, the fourth conductive layer is patterned to form interconnected lines the selectively connect the plurality of conductive vias. Yach et al. teach a plurality of capacitors can be connected through a interconnect line. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form an interconnect to connect a plurality of Watt capacitors; since such a modification would connect a plurality of like capacitors together providing a particular capacitance for a system.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Naito et al. (EP 0, 917,165 A2) in view of Yach et al. (US 6,225,678).

Naito et al. disclose the claimed invention except for a fourth conductive layer located over the third insulator layer, the fourth conductive layer is patterned to form interconnected lines the selectively connect the plurality of conductive vias. Yach et al. teach a plurality of capacitors can be connected through a interconnect line. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form an interconnect to connect a plurality of Naito et al. capacitors; since such a modification would connect a plurality of like capacitors together providing a particular capacitance for a system.

Claims 18, & 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farooq et al in view of Yach et al. (US 6,225,678).

Regarding claims 18, & 20, Farooq et al. disclose the claimed invention except for a fourth conductive layer located over the third insulator layer, the fourth conductive layer is patterned to form interconnected lines the selectively connect the plurality of conductive vias. Yach et al. teach a plurality of capacitors can be connected through a interconnect line. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form an interconnect to connect a plurality of Farooq et al. capacitors; since such a modification would connect a plurality of like capacitors together providing a particular capacitance for an electrical system.

Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Farooq et al.

Farooq et al. disclose the claimed invention except for the insulators are fabricated by a BaSrTiO<sub>3</sub> material. BaSrTiO<sub>3</sub> is a well known dielectric (insulator) used

in the capacitor art. It would have been obvious to one having ordinary skill in the art at the time the invention was made to form the insulators of Farooq et al. using BaSrTiO<sub>3</sub>, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416.

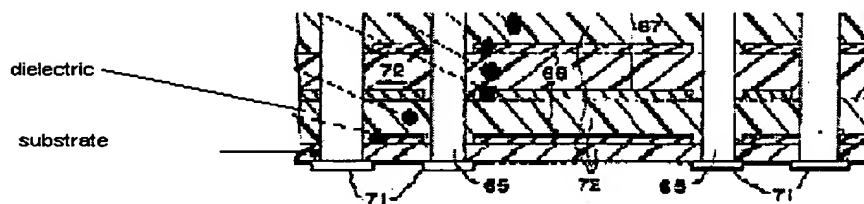
## Response to Arguments

Applicant's arguments with respect to claims 14-18 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments filed 8/20/01 have been fully considered but they are not persuasive.

## Farooq et al.

A) The argument "In the office action, element 72 of Farooq et al. is characterized as both a "substrate" and an insulator layer. However, as illustrated in the instant application (Figure 1, elements 202 and 208, respectively)... the substrate and dielectric are two distinct components." is confusing. Farooq clearly illustrates two separate distinct components; one being a substrate (72 -- an underlying layer) and the other a dielectric (72) separating two conductive layers.

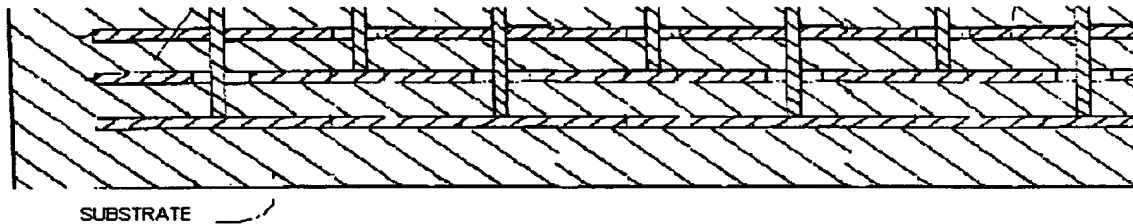


B) In response to applicant's argument that the references fail to show certain features of applicant's invention, it is noted that the features upon which applicant relies (i.e., The substrate is a layer through which conductive vias do not extend) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

C) The argument "it should be noted that it would be impossible to fabricate C4 lands "on" the third insulator layer, as claimed by the Applicant using the embodiment disclosed by Farooq et al. in Fig. 3C." is not persuasive. Applicant is reminded that the word "on" does not mean "directly in contact with". Farooq discloses a plurality of controlled collapse chip connection (C4) lands fabricated on the third insulator layer and in electrical contact with the plurality of conductive vias (col. 3 lines 25-30).

**Naito et al.**

A) The argument "in the Office action, it is also asserted that Naito et al. discloses a substrate. However, Fig. 1 of Naito et al. only recites and illustrates element 32, described as a dielectric material layer". Such a continuous dielectric layer is not the same as a substrate, upon which dielectric material and conductive material maybe formed" is not persuasive. Naito et al. clearly illustrates an underlying layer (substrate see fig. below)



### **Watt**

A) The argument "the office action asserts that "Watt discloses in Fig. 1a... substrate (1, 2); a first conductive layer 7 located over the substrate..." However, ... a substrate is not the same as a dielectric layer. In this case, layer "2" (element 14) of fig. 2 is an insulation layer formed over a substrate as claimed. Thus the insulation layer is not a substrate, being separate and distinct from the substrate, and the conductive layer is not located "over" the substrate, as claimed by the Applicant. Watt does not disclose a conductive layer located "over" a substrate" is not persuasive. Watt clearly illustrates two layers form an underlying layer (a substrate) in which the first conductive layer is located "over" the substrate. \*\*It should be noted that "over" does not mean directly in contact with.

### **(35 USC 103) Naito et al. in view of Farooq et al.**

A) Applicant is reminded that using C4 lands in the fabrication of capacitors is well known in the art. C4 connections are known to prevent a capacitor from collapsing onto a printed circuit.

### **(35 USC 103) Naito et al. & (35 USC 103) Farooq et al.**

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A) "Applicant objects to such official notice using a single reference and respectfully request that additional references be cited in support of this position"

Strontium Barium Titanate (SBT) is a well-known dielectric material used in the capacitor art. SBT is known for its high dielectric constant. See US 5,679,980; 5,793,057; 5,811,851; 5,781,404; 5,729,054; & 5,696,018.

Copper is a well-known electrode material. Copper has excellent electro-conductivity. See 5,910,881; 5,471,363; 5,512,353 5,093,757; 5,159,524; 5,117,326; 5,107,394; & 6,101,693.

**(35 USC 103) Watt in view of Yach et al.**

A) The argument "Yach et al. is directed to connecting capacitors to form a matched array. Watt recites only a single capacitor. One of ordinary skill in the art would not be moved to make a "matched array" of capacitors using the mesa-configuration of Watt. " is not persuasive. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form an interconnect to connect a plurality of



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Watt capacitors; since such a modification would connect a plurality of like capacitors together providing an increased capacitance for an electrical system.

**(35 USC 103) Naito et al. in view of Yach et al.**

A) In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to form an interconnect to connect a plurality of Naito capacitors; since such a modification would connect a plurality of like capacitors together providing an increased capacitance for an electrical system.

**(35 USC 103) Farooq et al. in view of Yach et al.**

A) In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, it would have

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been obvious to a person of ordinary skill in the art at the time the invention was made to form an interconnect to connect a plurality of Farooq capacitors; since such a modification would connect a plurality of like capacitors together providing an increased capacitance for an electrical system.

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric W Thomas whose telephone number is (703) 305-0878. The examiner can normally be reached on Mon & Sat 9:00 AM - 9:30 PM; Tue-Fri 5:30PM-10:00PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean Reichard can be reached on 703-308-3682. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-1341 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

ewt  
November 1, 2001

**ANTHONY DINKINS  
PRIMARY EXAMINER**

A handwritten signature in black ink, appearing to read "Anthony Dinkins", is written over a rectangular stamp area.